UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,435	12/23/1999	MICHAEL J. MCTAGUE	INTL-0296-US	7390

7590 04/22/2005

TIMOTHY N TROP
TROP PRUNER HU & MILES PC
8554 KATY FREEWAY
SUITE 100
HOUSTON, TX 77024

EXAMINER	
TRAN, KHANH C	
ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 09/471,435	Applicant(s) MCTAGUE ET AL.	
	Examiner Khanh Tran	Art Unit 2631	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 29 March 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1,3-7,9-15,17-28 and 30*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

TESFALDET BOCURE
PRIMARY EXAMINER

Continuation of 11. does NOT place the application in condition for allowance because:

Referring to page 2 of Reply to Final Rejection,
Applicants argue that "Neither of the cited references teach a multiplexer to multiplex said lower data rate data and control information and transmit the data and control information externally of said integrated circuit. With respect to the reference to Yukutake, it appears that the Examiner is taking the position that somehow the use of the isolators 501 and 502, in figure 1, teach the use separate circuits. But, even if one were to accept this relatively unsual position, it still fails to meet the claimed invention".

Examiner's position is that in rejecting claims 1, 3-7, 9-10, 14-15, 17, 20-23, 25-26, 28 and 30, the Examiner relies on the main reference, Kanekawa et al. U.S. 6,389,063 B1 to teach most of the claimed features [Emphasis added]. Contrary to the Applicants' argument "Neither of the cited references teach a multiplexer to multiplex said lower data rate data and control information and transmit the data and control information externally of said integrated circuit", as recited in the Final rejection and repeating again, figure 23 shows a constitution of AFE 100, wherein a clock signal CLK inputted from the host side is transmitted the subscriber line side via an isolating capacitor 2-0 of an isolator 50-0. Control circuits 101 and 102 exchange necessary control information via isolators 2-1 and 2-2 of isolators 50-1 and 50-2. Since isolators 50-2, 50-1 and 50-2 could be formed on monolithic integrated circuits and electrically separating and insulating AFE 100, AFE 100 effectively forms two separate regions, constituting equivalent first and second integrating circuits as claimed in the pending application. The first region connecting to the subscriber line side includes an analog-to-digital converter (ADC) 105 producing data at a relatively higher data rate data due to oversampling, a multiplexer 111 for multiplexing the data rate data and coded control information from the control circuit 101. The first region also includes a demultiplexer 113 for demultiplex the data rate data and coded control information from the control circuit 102 from a second region. The second region, connecting to the host side (see also figure 20), includes a demultiplexer 112 for demultiplexing the data rate data and control information, and a low-pass filter and decimator 106 for reducing the data rate data. The second region also includes a multiplexer 114 for multiplexer the data rate data and coded control information from the control circuit 102. In column 13, lines 1-35, Kanekawa et al. further teach that in the oversampling system, the digital signal is thinned down (e.g. data rate reduced) by a low-pass filter (LPF) and decimator (DCM) 106 to a signal at a low sampling frequency and outputted to the host side. On the other hand, signal is inputted from the host as a digital signal and in the oversampling system, it is interpolated to a signal at the oversampling frequency by a low-pass filter and interpolator 110.

In column 13, lines 30-36, Kanekawa further teaches that if sending and receiving data and control information are switched and transmitted on a time-shared basis by multiplexers (MUX) 111 and 114 and a demultiplexer (DEMUX) 112, the number of necessary isolators and isolating capacitors thereof can be reduced. As recited in the Final rejection, although Kanekawa teaches a low pass filter and decimator 106 for reducing the data rate data, however, the arrangement of the low pass filter and decimator 106 is not between ADC 105 and MUX 111 as claimed in the pending application. For that reason, the Examiner relies on a secondary reference, Yukutabe et al. US 6,603,807 B1, to show that a decimator can be arranged on the same side and located between ADC 105 and MUX 111. Return to the embodiment of figure 23 of Kanekawa invention, low-pass filter and decimator 106 is there to reduce the data rate data being oversampled by ADC 105 as taught in the invention [Emphasis added]. In view of that, one of ordinary skill in the art would have recognized that low-pass filter and decimator 106 can be anywhere after ADC 105. Because Yukutabe et al. teachings further disclose that a decimator 515 can be located after ADC 514 to reduce the data rate data before transmitting to the second region via isolator 502, it would have been obvious for one of ordinary skill in the art at the time of invention Kanekawa teachings can be modified to implement a low-pass filter and decimator 106 after ADC 105 and before MUX 111. As recited above, MUX 111 (see figure 23) is for sending data and control information are transmitted on a time-shared basis. The arrangement of low-pass filter and decimator 106 before MUX 111 has no effect on the operation of MUX 111.

In further recited in the Final rejection, Examiner's position is that as expressly taught in Kanekawa et al. invention, isolating capacitors 2-0 2-1 ... of an isolators 50-0 50-1 50-2 ... are employed to isolate the region on the host side from the subscriber line side; see column 12 line 25 through column 13 line 35, see also figures 21 22 23. Similarly, in column 8, lines 45-67, Yukutake et al. teaches the layout as shown in figure 2, the circuit areas 601 602 603 are enclosed by trenches so as to form an analog I/O side circuit area 601, an isolator area 602, and a digital I/O side circuit area 603. By enclosing each circuit block in the circuit areas 601 to 603, the circuits are insulated and separated from each other and the devices are separated [Emphasis added]. Due to the layout as shown in figure 2 of Yukutake et al. invention, the circuit areas 601 602 603 are separate areas and insulated from each other. And as recited above, because the isolator area 602 can be implemented on a monolithic integrated circuit, one of ordinary skill in the art of IC technology would have been motivated to implement the circuit areas 601 and 603 on separate integrated circuits. As further discussed in Summary of Yukutake et al. invention in column 3 lines 20-31, an object of Yukutake et al. teachings is to realize an IC isolator using the monolithic insulating barrier, IC application circuits, IC line interface or an analog front end (AFE) including an interface or conversion circuits for analog and digital circuits. The conversion circuits for analog and digital circuits would qualify as IC application circuits, also known as chips. The benefits of using separate chips (IC circuits) are to make the design highly modular as appreciated by a person of average skill in the art of integrated circuit technology. The motivations for isolating and separating the regions are inventive features of Yukutake et al. and Kanekawa et al. teachings.

The Examiner emphasizes that introduction of Yukutabe et al. invention is to show the decimator can be implemented after ADC 105 of the first region in Kanekawa invention, and to further support that analog I/O side circuit area and digital I/O side circuit area of AFE 100 (see figure 23) in Kanekawa invention can be implemented on separate integrated circuits. With the modification of Kanekawa teachings, referring to figure 23, MUX 111 multiplexes lower data rate data with control information and transmit lower data rate data and control information from the first region to the second region as claimed in the pending application.

The Examiner strongly disagees with Applicants' arguments on the secondary reference, Yukutake invention, on page 2. As recited

again, introduction of Yukutabe et al. invention is to show the decimator can be implemented after ADC 105 of the first region in Kanekawa invention, and to further support that analog I/O side circuit area and digital I/O side circuit area of AFE 100 (see figure 23) in Kanekawa invention can be implemented on separate integrated circuits. The Examiner relies on the main reference, Kanekawa invention, to show all claimed limitations, but the arrangement of low-pass filter and decimator 106. However, with Yukutake teachings, it would have been obvious for one of ordinary skill in the art at the time of invention that Kanekawa teachings can be modified to teach the missing features. The motivation for combining Kanekawa and Yukutake teachings is set forth in the Final rejection.